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SEMICONDUCTOR DEVICE

Inventor:	Shuzo Ito Rohm Co., Ltd. 21 Saiin, Mizosaki-cho, Ukyo-ku, Tokyo
Applicant:	000116024 Rohm Co., Ltd.

21 Saiin, Mizosaki-cho,
Ukyo-ku, Tokyo

Agent: Kosaku Ineoka,
patent atorney,
and 2 others

[There are no amendments to this patent.]

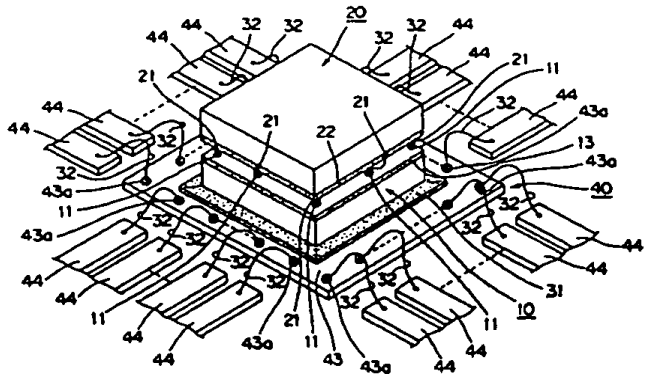
Abstract

Objective

To provide a semiconductor device capable of further improving the integration and easily realize an element having a new function.

Constitution

IC chip (10) is bonded to header (43) of lead frame (40) in a state of having faced the circuit forming surface upward and input/output pat [sic; pad] (43a) of header (43) and lead (44) are bonded. Solder chip (21) of IC chip (20) is placed on solder bump (11) of IC chip (10) in a state of having faced the circuit forming surface downward, IC chips (20) is superimposed on IC chip (10), then resin sealed.



Key: 10,20 IC chip
11,21 Solder bump
13,23 Insulating film
31 Adhesive
32 Bonding wire
40 Lead frame
43 Header
44 Lead
43a Input/output pat

Claims

1. A semiconductor device characterized by the fact that it is a semiconductor device composed by superimposing a plurality of integrated circuit chips,

solder bump is formed respectively at the superimposing surface of the integrated circuit chip to be superimposed at a position based on the integrated circuit design and a position which gave consideration to the to be superimposed integrated circuit chip, and the integrated circuit chips are mutually connected by the solder bumps being mutually bonded.

2. A semiconductor device characterized by the fact that it includes a first integrated circuit which is arranged with the circuit forming surface facing upward and the circuit forming surface is covered with an insulating film,

a second integrated circuit chip which is arranged with the circuit forming surface facing downward, at least one part of the circuit forming surface is opposed to the circuit forming surface of the first integrated circuit chip, and the circuit forming surface is covered with an insulating film, and

a connecting means which has plural solder bumps for maintaining the first integrated circuit chip and the second integrated circuit chip at a prescribed spacing and physically and electrically connects the predetermined position of the circuit forming surface of the first integrated circuit chip and the predetermined position of the circuit forming surface of the second integrated circuit chip by permeating the insulating films of the integrated circuit chips.

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